類比積體電路實習心得報告:

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學號:108360133

1. 心得:

一開始我以為類比積體電路設計就是接電路而已，並沒有什麼需要動腦的地方，單存按圖施工就好；但等到開始學習時，才發現原來是用程式來模擬電路。在接觸這堂課快一個學期了，很感謝陳建中老師教我們需多丁組需要用到的知識，老師有說過如果認真把這門課學會基本上去業界會比較輕鬆；雖然這門課快結束了，但我一定會再找時間把她讀透的(為了在業界比較輕鬆)。

二`上課內容:

LAB1

ROSC

.lib 'C:\sp\cic018.l' tt

.SUBCKT INV 10 20 100 99

M1 20 10 100 100 P\_18 W=2U L=2U

M2 20 10 99 99 N\_18 W=1U L=2U

.ENDS INV

.SUBCKT NAND A B Y 100 99

M1 Y A 100 100 P\_18 W=1u L=2u

M2 Y B 100 100 P\_18 W=1u L=2u

M3 Y B 1 99 N\_18 W=2u L=2u

M4 1 A 99 99 N\_18 W=2u L=2u

.ENDS NAND

.SUBCKT NOR A B Y 100 99

M1 1 A 100 100 P\_18 W=2u L=2u

M2 Y B 1 100 P\_18 W=2u L=2u

M3 Y A 99 99 N\_18 W=1u L=2u

M4 Y B 99 99 N\_18 W=1u L=2u

.ENDS NOR

Vdd 100 0 dc PWL(0 0 1us 0 1.1us 1.8V 2us 1.8V)

\*X1 1 2 101 98 INV

\*X2 2 3 101 98 INV

\*X3 3 4 101 98 INV

\*X4 4 5 101 98 INV

\*X5 5 1 101 98 INV

\*Mx1 20 20 100 100 P\_18 W=2u L=0.2u

\*Mx2 21 21 0 0 N\_18 W=1u L=0.2u

\*Mx3 101 20 100 100 P\_18 W=2u L=0.2u

\*Mx4 98 21 0 0 N\_18 W=1u L=0.2u

\*Ix1 20 21 DC 10uA

X1 1 1 2 101 98 NAND

X2 2 2 3 101 98 NAND

X3 3 3 4 101 98 NAND

X4 4 4 5 101 98 NAND

X5 5 5 1 101 98 NAND

My1 22 22 100 100 P\_18 W=2u L=0.2u

My2 23 23 0 0 N\_18 W=1u L=0.2u

My3 101 22 100 100 P\_18 W=2u L=0.2u

My4 98 23 0 0 N\_18 W=1u L=0.2u

Iy1 22 23 DC 1uA

\*X1 1 1 2 101 98 NOR

\*X2 2 2 3 101 98 NOR

\*X3 3 3 4 101 98 NOR

\*X4 4 4 5 101 98 NOR

\*X5 5 5 1 101 98 NOR

\*Mz1 24 24 100 100 P\_18 W=2u L=0.2u

\*Mz2 25 25 0 0 N\_18 W=1u L=0.2u

\*Mz3 101 24 100 100 P\_18 W=2u L=0.2u

\*Mz4 98 25 0 0 N\_18 W=1u L=0.2u

\*Iz1 24 25 DC 1uA

\*\*analysis

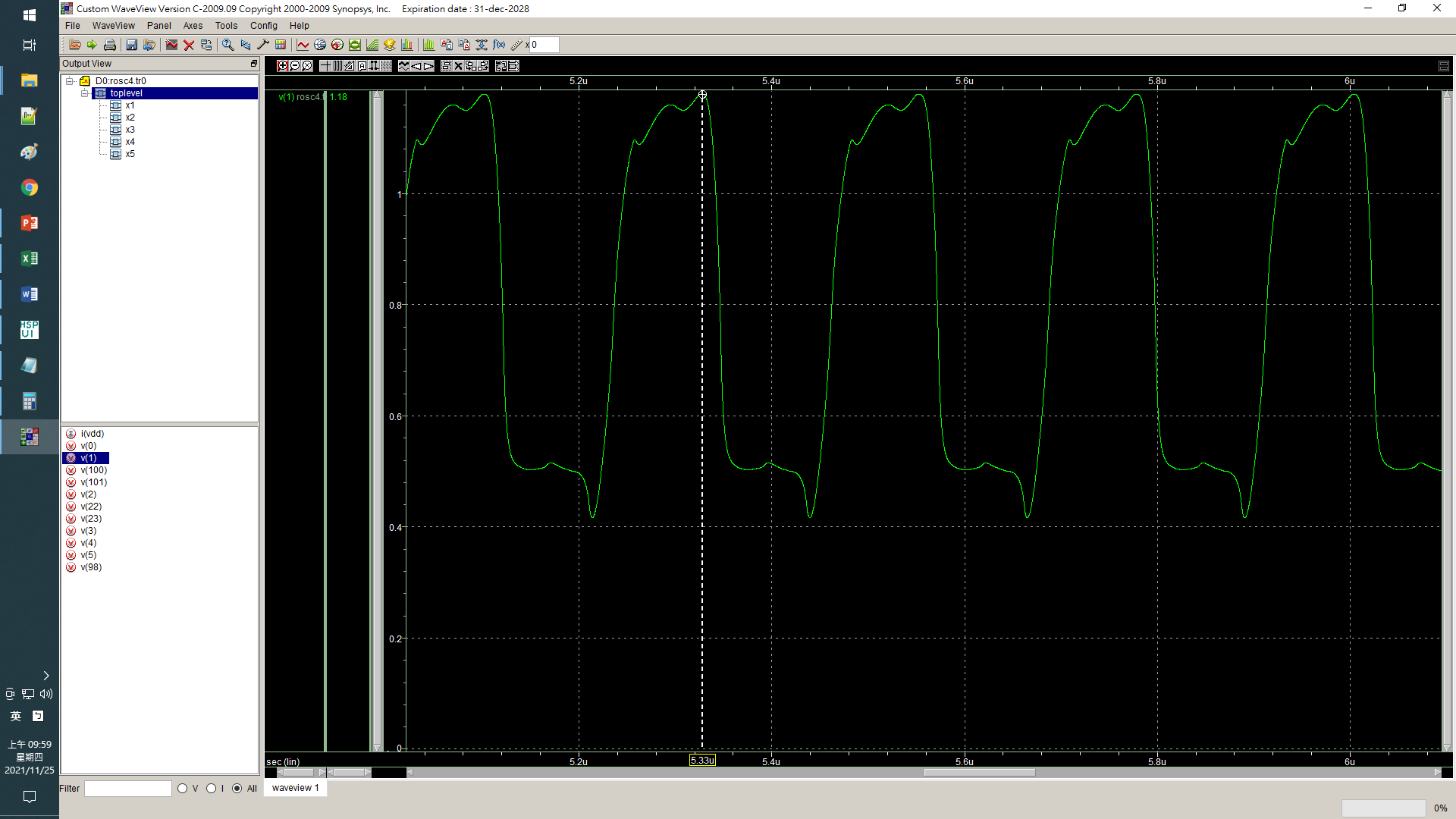
.op

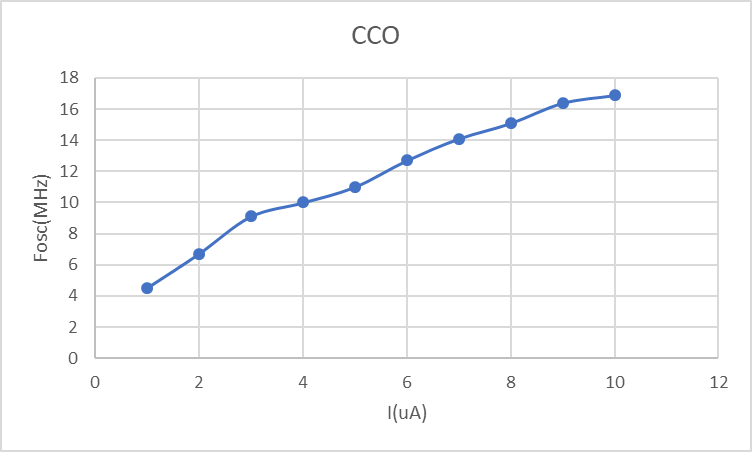
.option post

.tran 1ps 10us 0 0.1ns

.probe

.end





**LAB2**

ROSC

.lib 'C:\sp\cic018.l' tt

.SUBCKT INV 10 20 100 99

M1 20 10 100 100 P\_18 W=2U L=2U

M2 20 10 99 99 N\_18 W=1U L=2U

.ENDS INV

.SUBCKT NAND A B Y 100 99

M1 Y A 100 100 P\_18 W=1u L=2u

M2 Y B 100 100 P\_18 W=1u L=2u

M3 Y B 1 99 N\_18 W=2u L=2u

M4 1 A 99 99 N\_18 W=2u L=2u

.ENDS NAND

.SUBCKT NOR A B Y 100 99

M1 1 A 100 100 P\_18 W=2u L=2u

M2 Y B 1 100 P\_18 W=2u L=2u

M3 Y A 99 99 N\_18 W=1u L=2u

M4 Y B 99 99 N\_18 W=1u L=2u

.ENDS NOR

Vdd 100 0 dc PWL(0 0 1us 0 1.1us 1.8V 2us 1.8V)

\*X1 1 2 101 98 INV

\*X2 2 3 101 98 INV

\*X3 3 4 101 98 INV

\*X4 4 5 101 98 INV

\*X5 5 1 101 98 INV

\*Mx1 20 20 100 100 P\_18 W=2u L=0.2u

\*Mx2 21 21 0 0 N\_18 W=1u L=0.2u

\*Mx3 101 20 100 100 P\_18 W=2u L=0.2u

\*Mx4 98 21 0 0 N\_18 W=1u L=0.2u

\*Ix1 20 21 DC 10uA

\*X1 1 1 2 101 98 NAND

\*X2 2 2 3 101 98 NAND

\*X3 3 3 4 101 98 NAND

\*X4 4 4 5 101 98 NAND

\*X5 5 5 1 101 98 NAND

\*My1 22 22 100 100 P\_18 W=2u L=0.2u

\*My2 23 23 0 0 N\_18 W=1u L=0.2u

\*My3 101 22 100 100 P\_18 W=2u L=0.2u

\*My4 98 23 0 0 N\_18 W=1u L=0.2u

\*Iy1 22 23 DC 1uA

X1 1 1 2 101 98 NOR

X2 2 2 3 101 98 NOR

X3 3 3 4 101 98 NOR

X4 4 4 5 101 98 NOR

X5 5 5 1 101 98 NOR

Mz1 24 24 100 100 P\_18 W=2u L=0.2u

Mz2 25 25 0 0 N\_18 W=1u L=0.2u

Mz3 101 24 100 100 P\_18 W=2u L=0.2u

Mz4 98 25 0 0 N\_18 W=1u L=0.2u

Iz1 24 25 DC 1uA

\*\*analysis

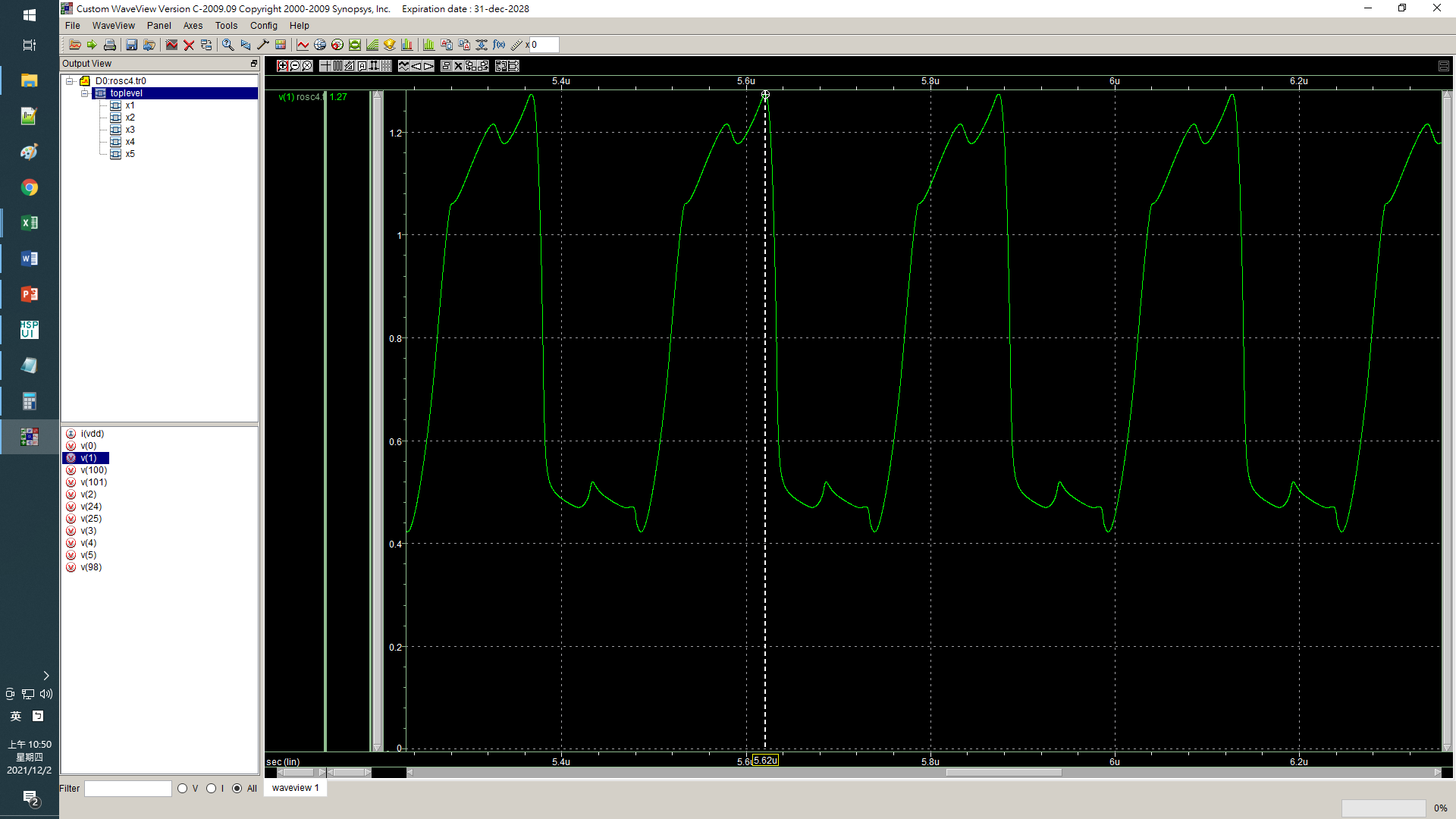
.op

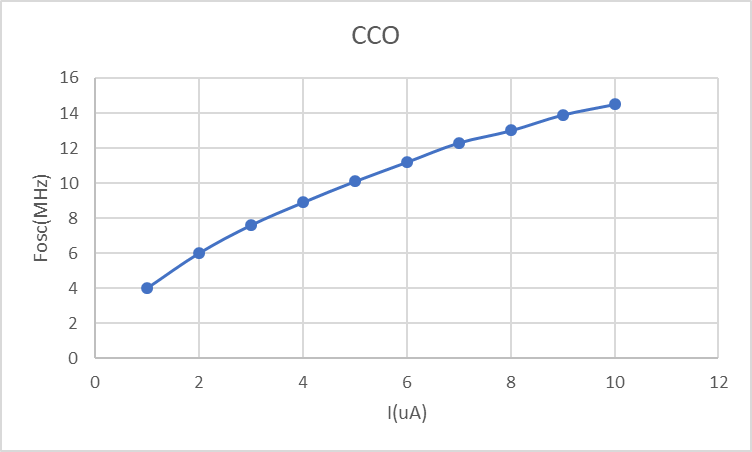
.option post

.tran 1ps 10us 0 0.1ns

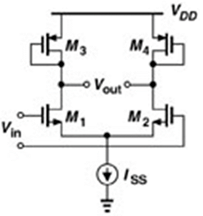
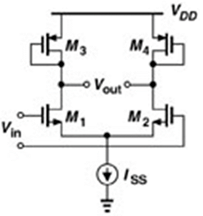
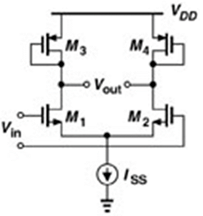
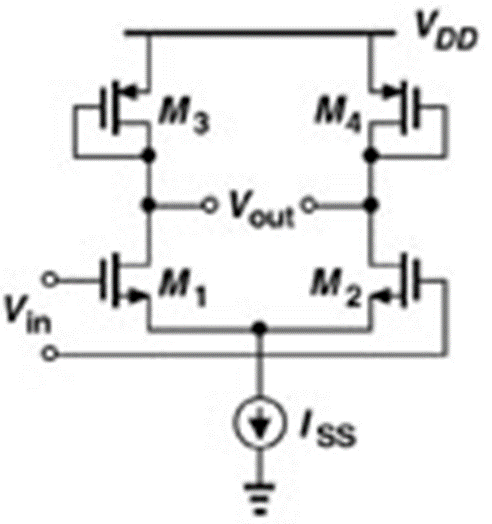
.probe

.end





**LAB3**



Cascaded Amplifier

.lib 'C:\sp\cic018.l' tt

.global gnd! vdd!

vdd vdd! 0 dc 1.8V

vss gnd! 0 dc 0

.SUBCKT DA Vinp Vinn 2 1 \*\*\*Voutp Voutn

M1 1 Vinp 3 gnd! N\_18 W=5u L=0.5u M=1

M2 2 Vinn 3 gnd! N\_18 W=5u L=0.5u M=1

M3 1 1 vdd! vdd! P\_18 W=1u L=0.5u M=1

M4 2 2 vdd! vdd! P\_18 W=1u L=0.5u M=1

M5 3 Vb gnd! gnd! N\_18 W=1u L=0.5u M=1

Vb Vb gnd! DC 0.65V

.ENDS DA

Vinp Vinp 0 DC 0.97V AC 0.5V sin(0.97V 0.5mV 1000k)

Vinn Vinn 0 DC 0.97V AC 0.5V 180 sin(0.97V 0.5mV 1000k 0 0 180)

X1 Vinp Vinn Voutp1 Voutn1 DA

X2 Voutp1 Voutn1 Voutp2 Voutn2 DA

X3 Voutp2 Voutn2 Voutp3 Voutn3 DA

X4 Voutp3 Voutn3 Voutp4 Voutn4 DA

\*\*analysis

.op

.option post

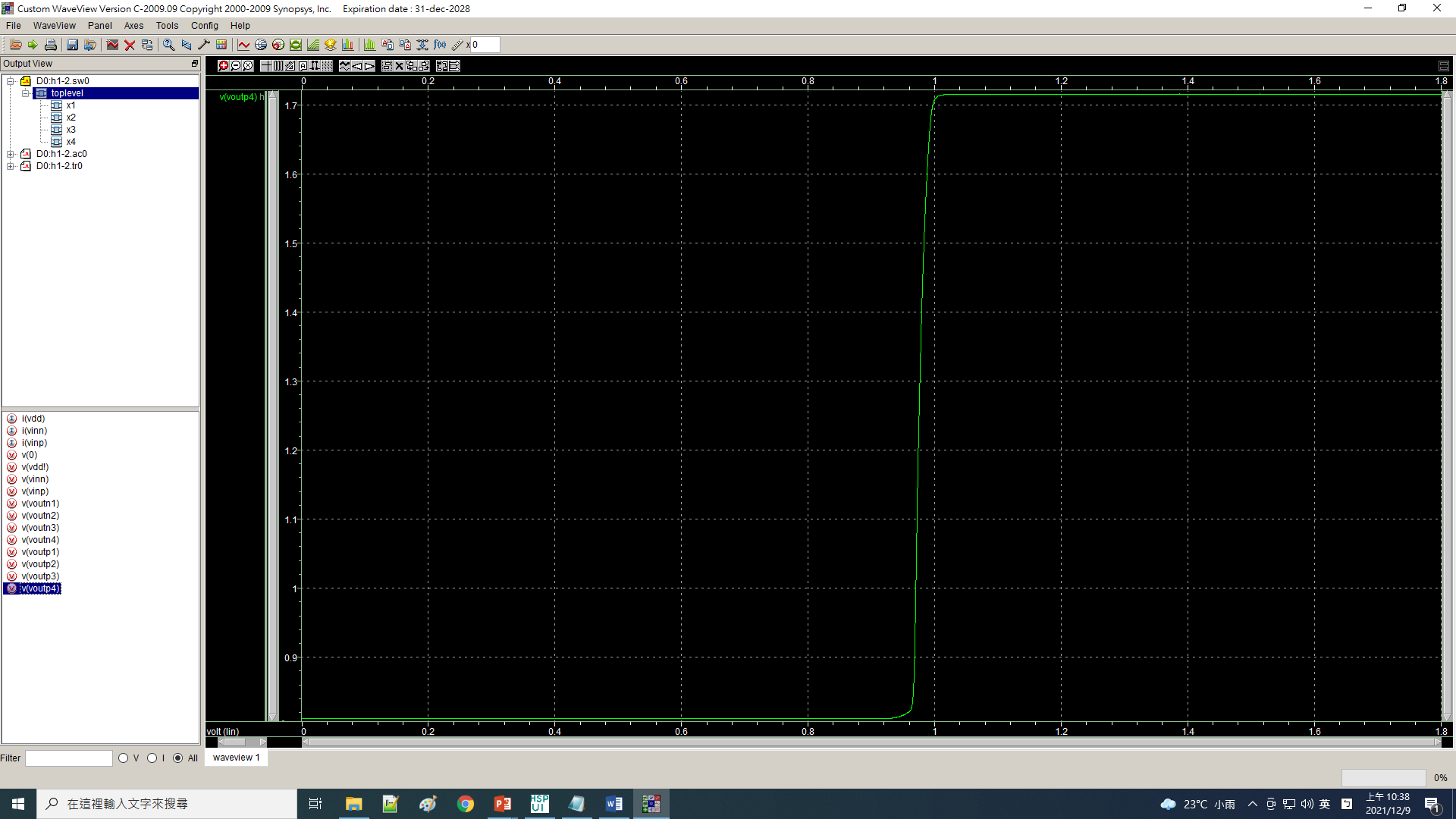
.ac dec 50 1 1g

.dc Vinp 0 1.8 0.0001

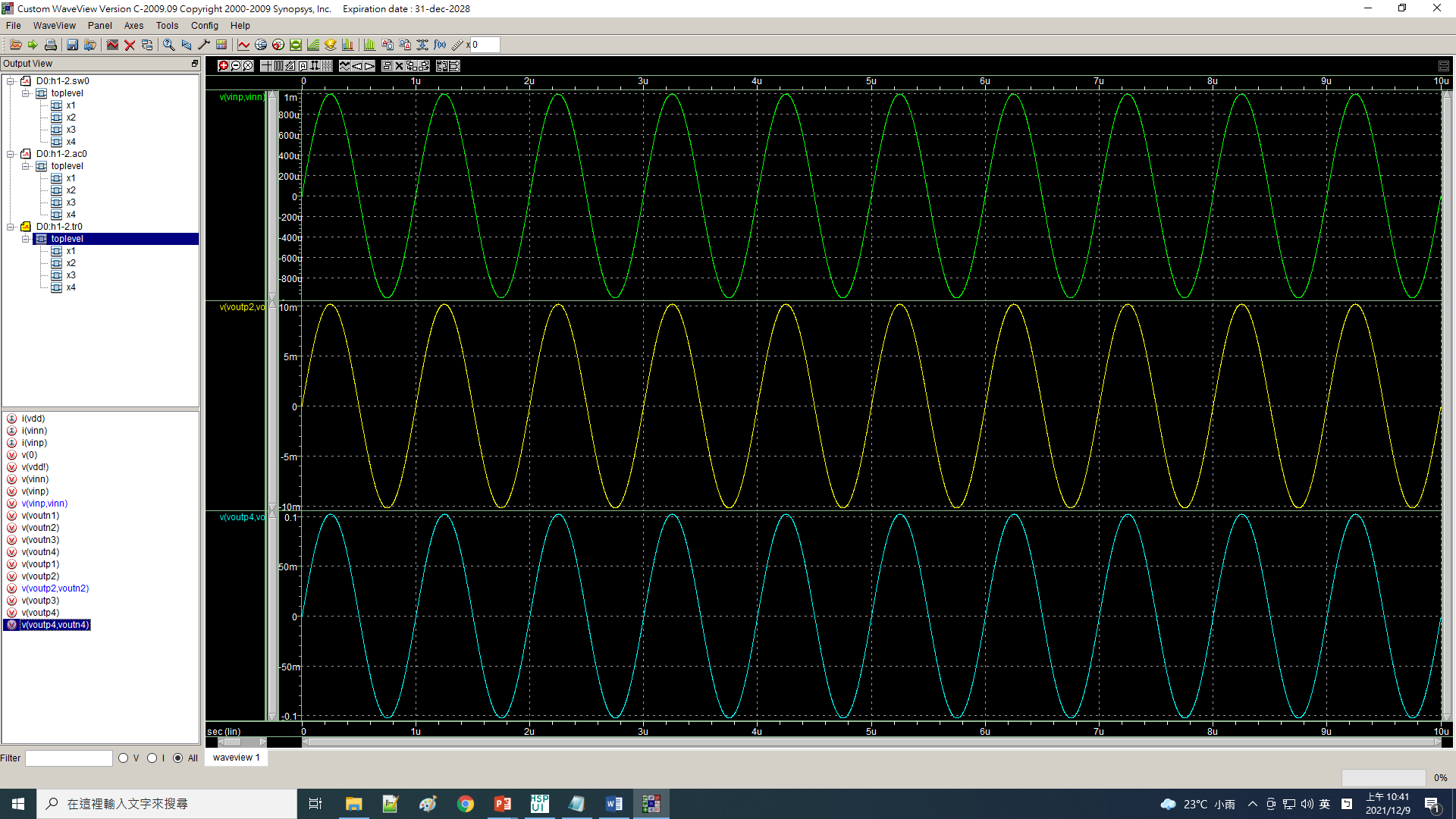
.tran 10ns 10us 0us 1ns

.probe V(voutp4, voutn4) V(vinp, vinn) V(voutp2, voutn2)

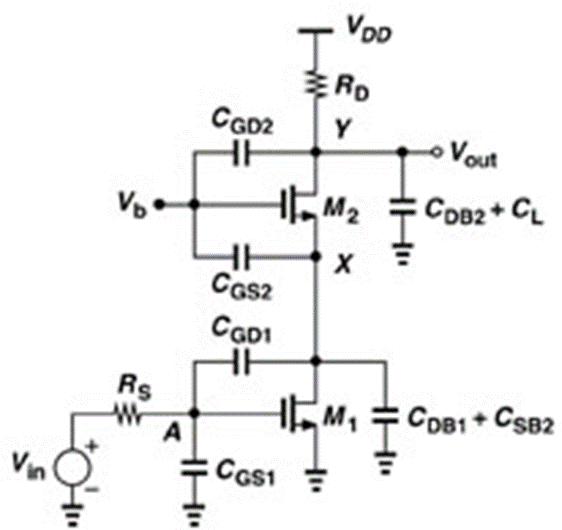
.end







**LAB4**



Cascoded Amplifier

.lib 'C:\sp\cic018.l' tt

.global gnd! vdd!

vdd vdd! 0 dc 1.8V

vss gnd! 0 dc 0

M2 Vout Vb X gnd! N\_18 W=5u L=0.2u M=36

M1 X A gnd! gnd! N\_18 W=5u L=0.2u M=14

Vin Vin 0 DC 0.589V AC 1V sin(0.589V 10mV 1000k)

Vb Vb 0 1.0V

Rs Vin A 1k

Rd Vdd! Vout 1k

\*\*analysis

.op

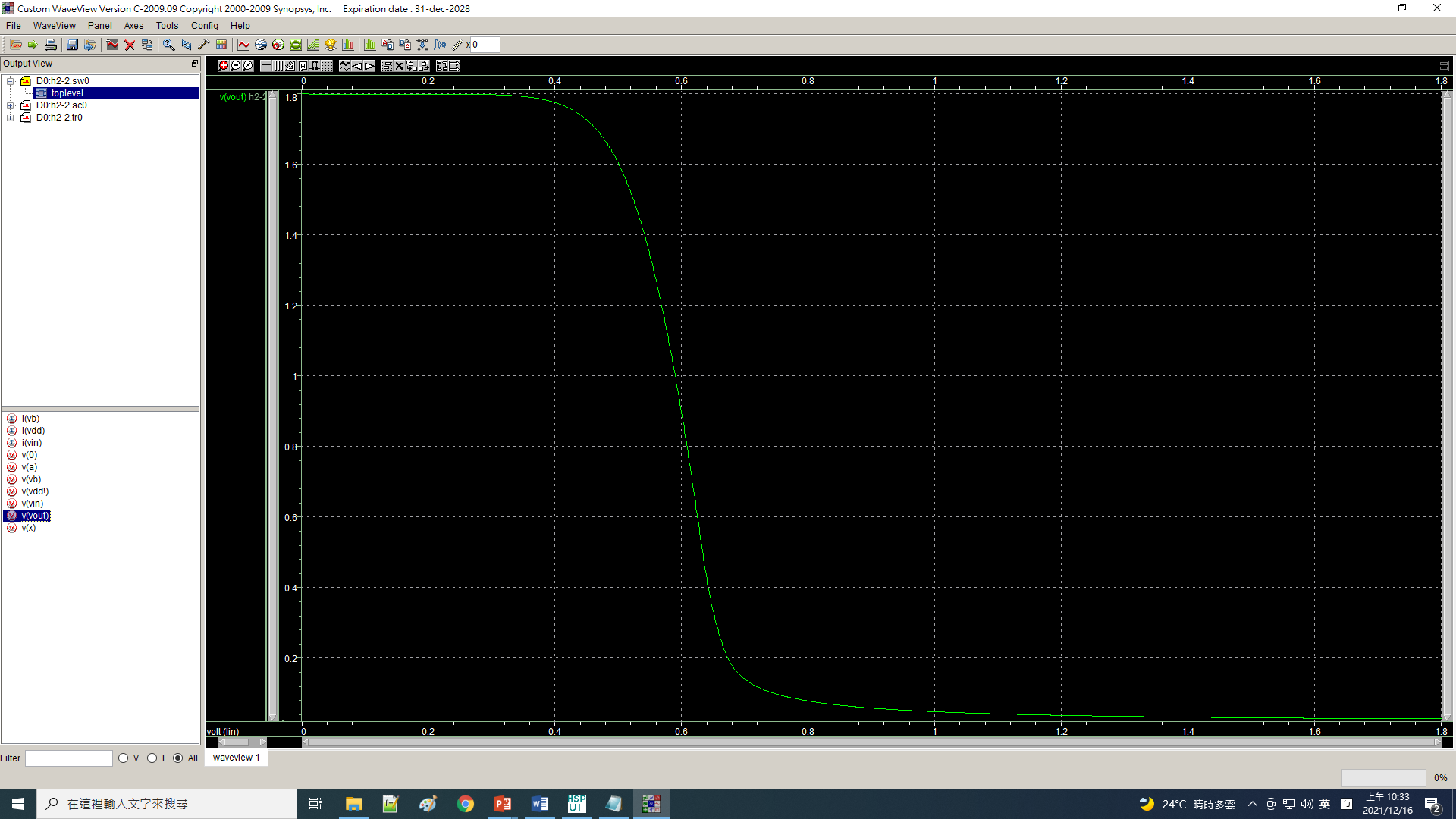
.option post

.ac dec 50 1 1g

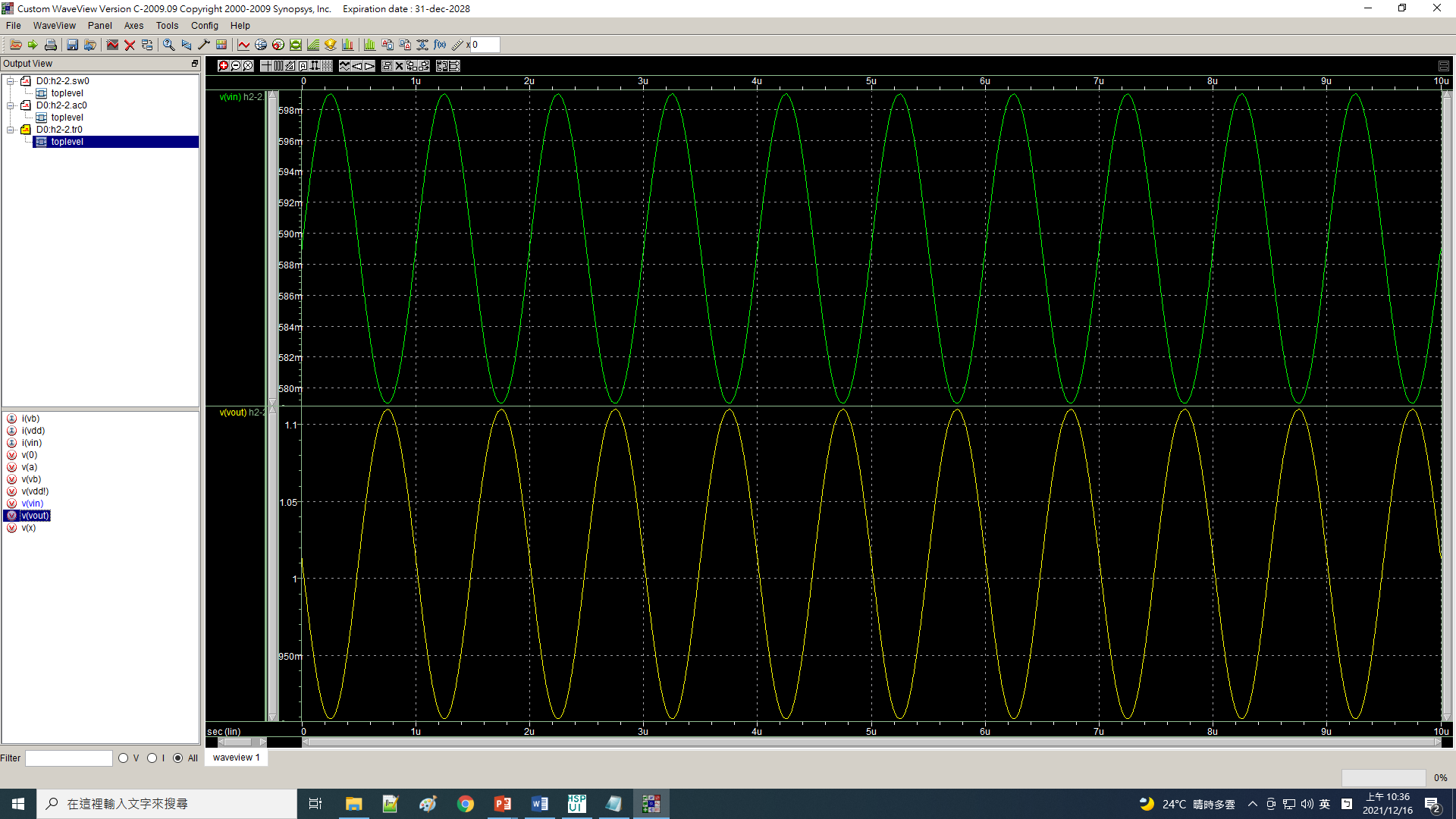
.dc Vin 0 1.8 0.001

.tran 10n 10u 0 10ns

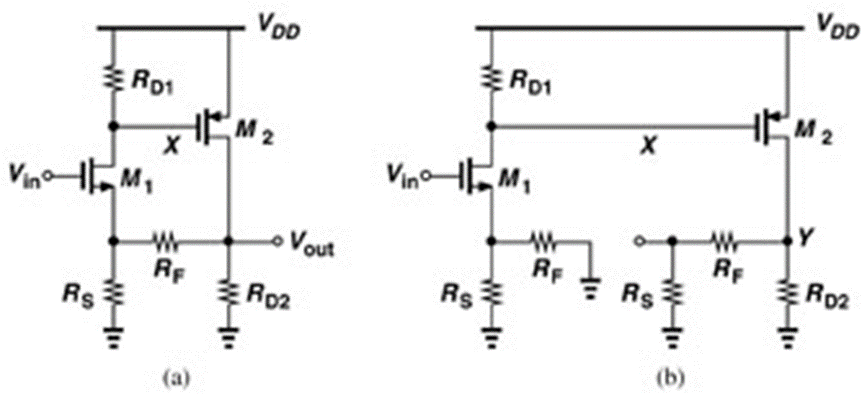
.end







**LAB5**



Feedback Amplifier

.lib 'C:\sp\cic018.l' tt

.global gnd! vdd!

M2 vout 1 vdd! vdd! p\_18 W=10u L=0.2u M=4

M1 1 vin 2 gnd! n\_18 W=10u L=0.2u M=1

Rd1 vdd! 1 2.2k

Rs 2 gnd! 1k

Rf 2 vout 50k

Rd2 vout gnd! 100k

vdd vdd! 0 dc 1.8V

vss gnd! 0 dc 0

vin vin 0 dc 0.874V ac 1V sin(0.874 50mV 1meg)

\*\*analysis

.op

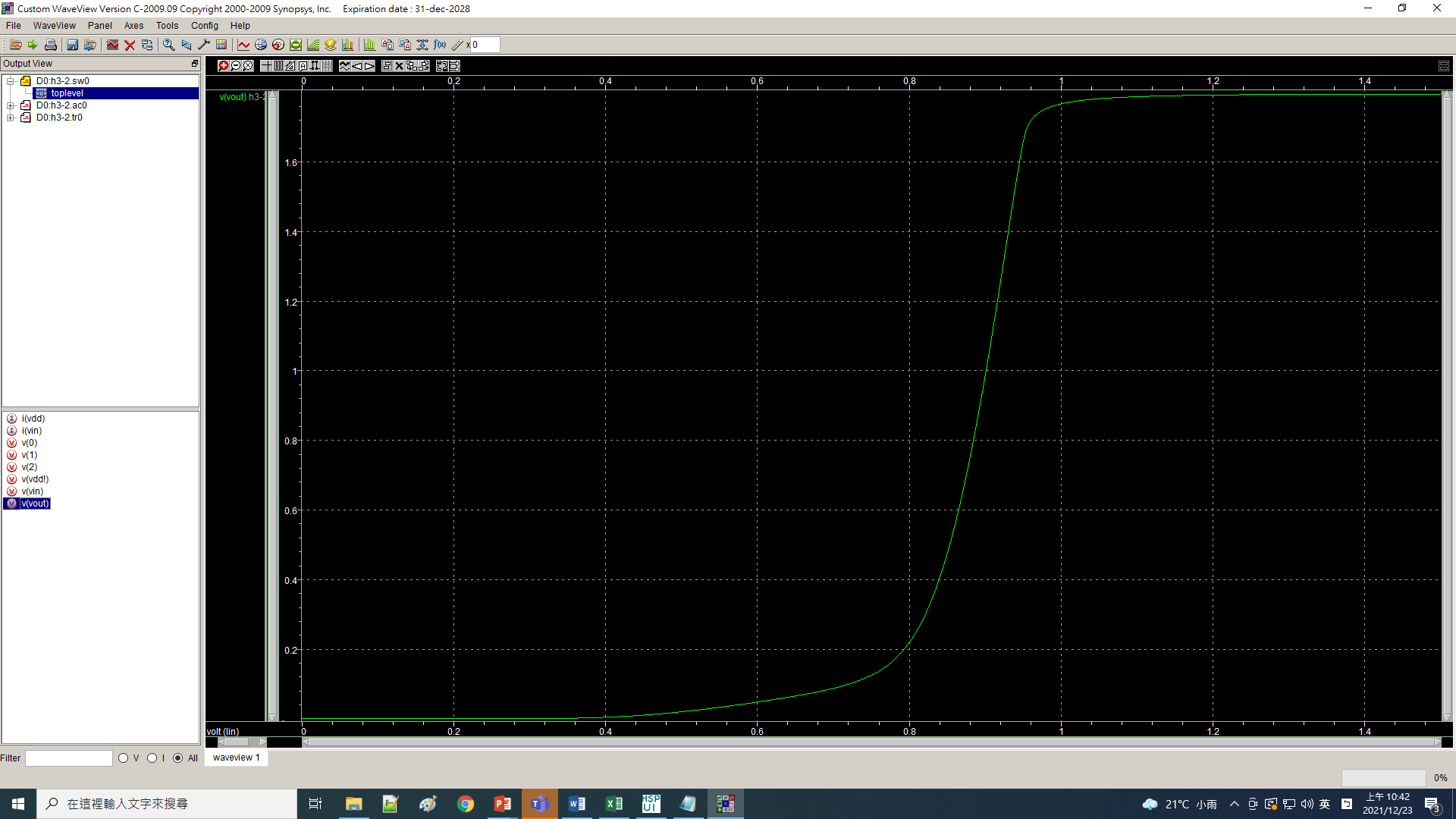
.option post

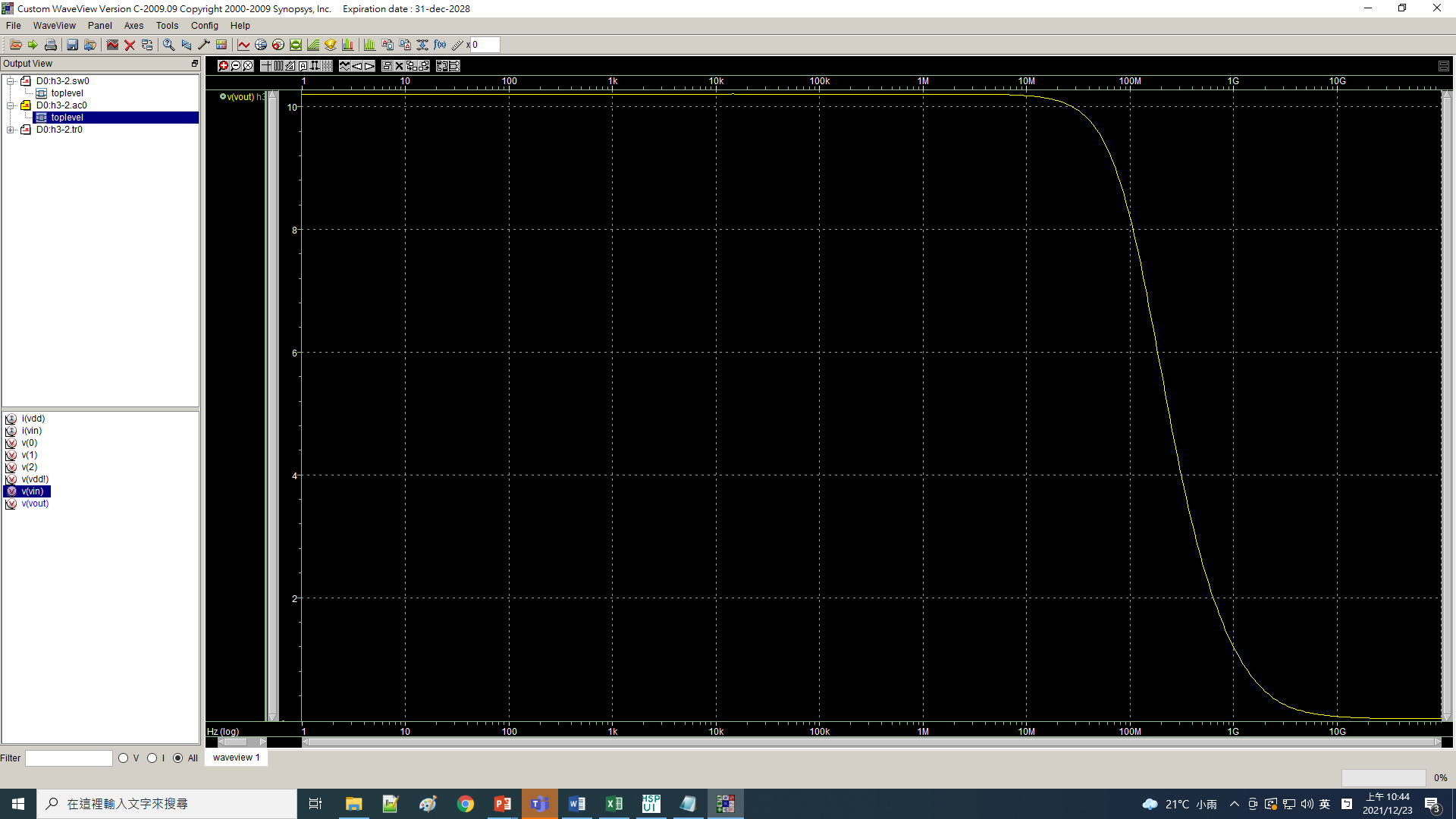
.dc vin 0 1.5 0.001

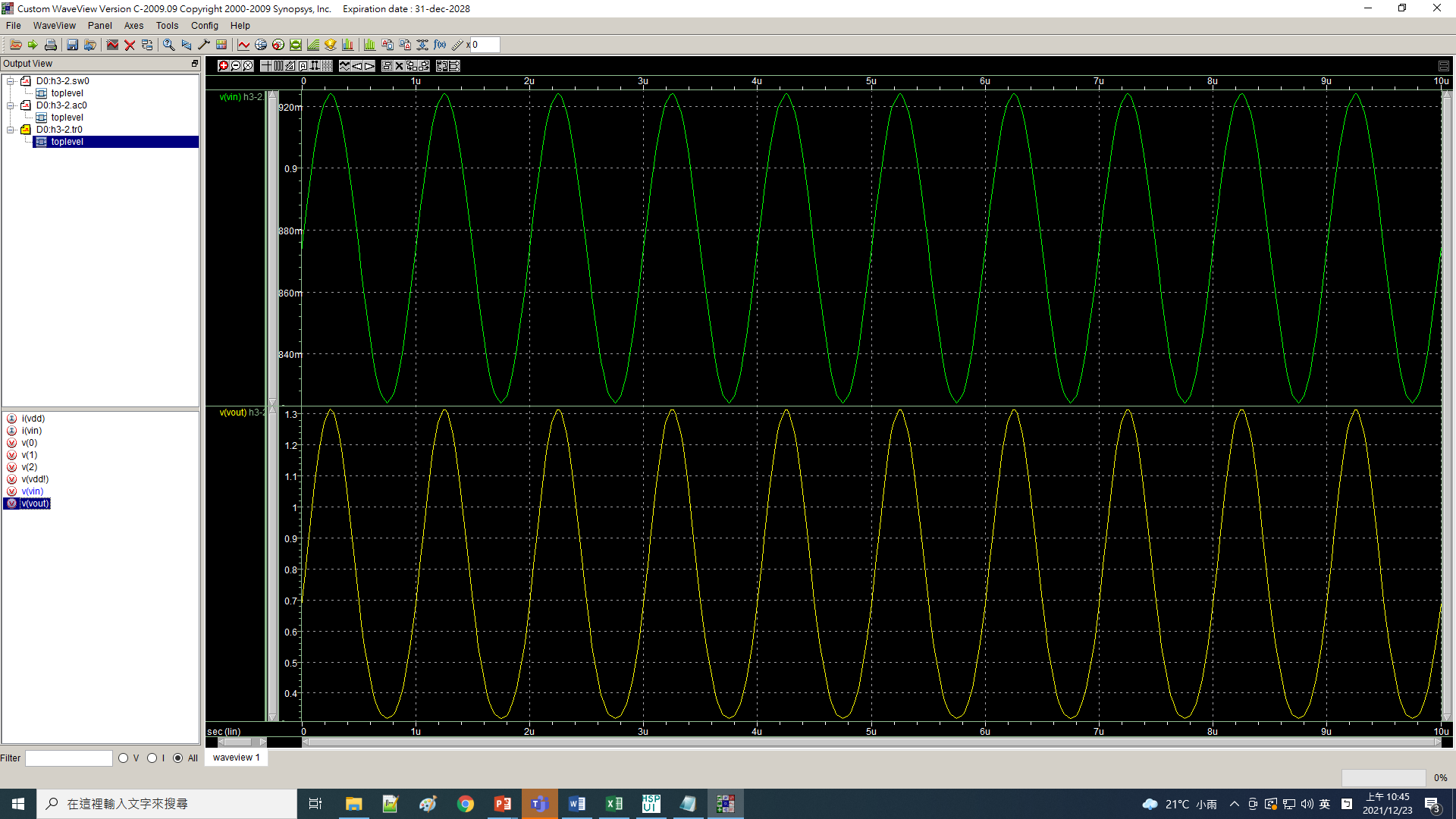
.tran 1ns 10us

.ac dec 50 1 100g

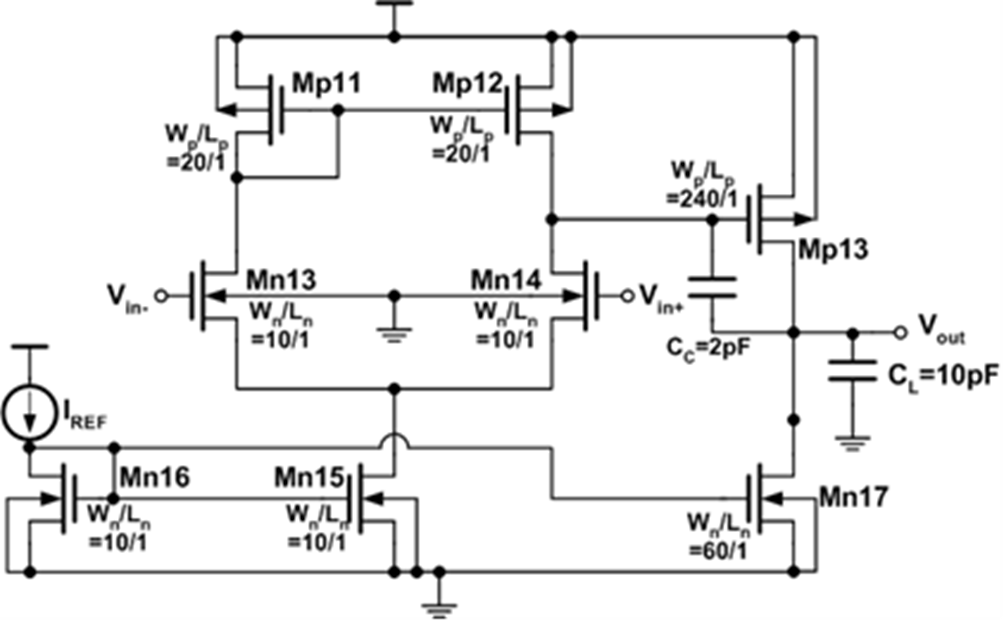
.end







**LAB6**



OPA

.lib 'C:\sp\cic018.l' tt

.global gnd! vdd!

vdd vdd! 0 dc 1.8V

vss gnd! 0 dc 0

m1 v1 vb vdd! vdd! p\_18 w=0.25u l=0.18u m=1

m2 v2 v2 vdd! vdd! p\_18 w=30u l=1u m=10

m3 v4 v2 vdd! vdd! p\_18 w=30u l=1u m=10

m4 vo v4 vdd! vdd! p\_18 w=19u l=1u m=10

m5 v2 vinn v3 gnd! n\_18 w=33u l=1u m=15

m6 v4 vinp v3 gnd! n\_18 w=33u l=1u m=15

m7 v1 v1 gnd! gnd! n\_18 w=25u l=1u m=3

m8 v3 v1 gnd! gnd! n\_18 w=50u l=1u m=15

m9 vo v1 gnd! gnd! n\_18 w=22u l=1u m=10

Vb Vb gnd! DC 0.4V

Cc vo v40 5p

Rc v40 v4 1k

\*Vinp Vinp 0 DC 1V AC 1V sin(0.9V 0.25V 1000k)

Vinp Vinp 0 DC 0.9V AC 0.5V sin(0.9V 50uV 1k)

Vinn Vinn 0 DC 0.9V AC 0.5V 180 sin(0.9V -50uV 1k)

\*R1 Vinn Vo 1

\*\*analysis

.op

.option post

.option acout=0

.dc Vinp 0 1.8 0.001

.ac dec 50 1 1g

\*.tran 10n 10u 0 10ns

.tran 10n 10m 0 10us

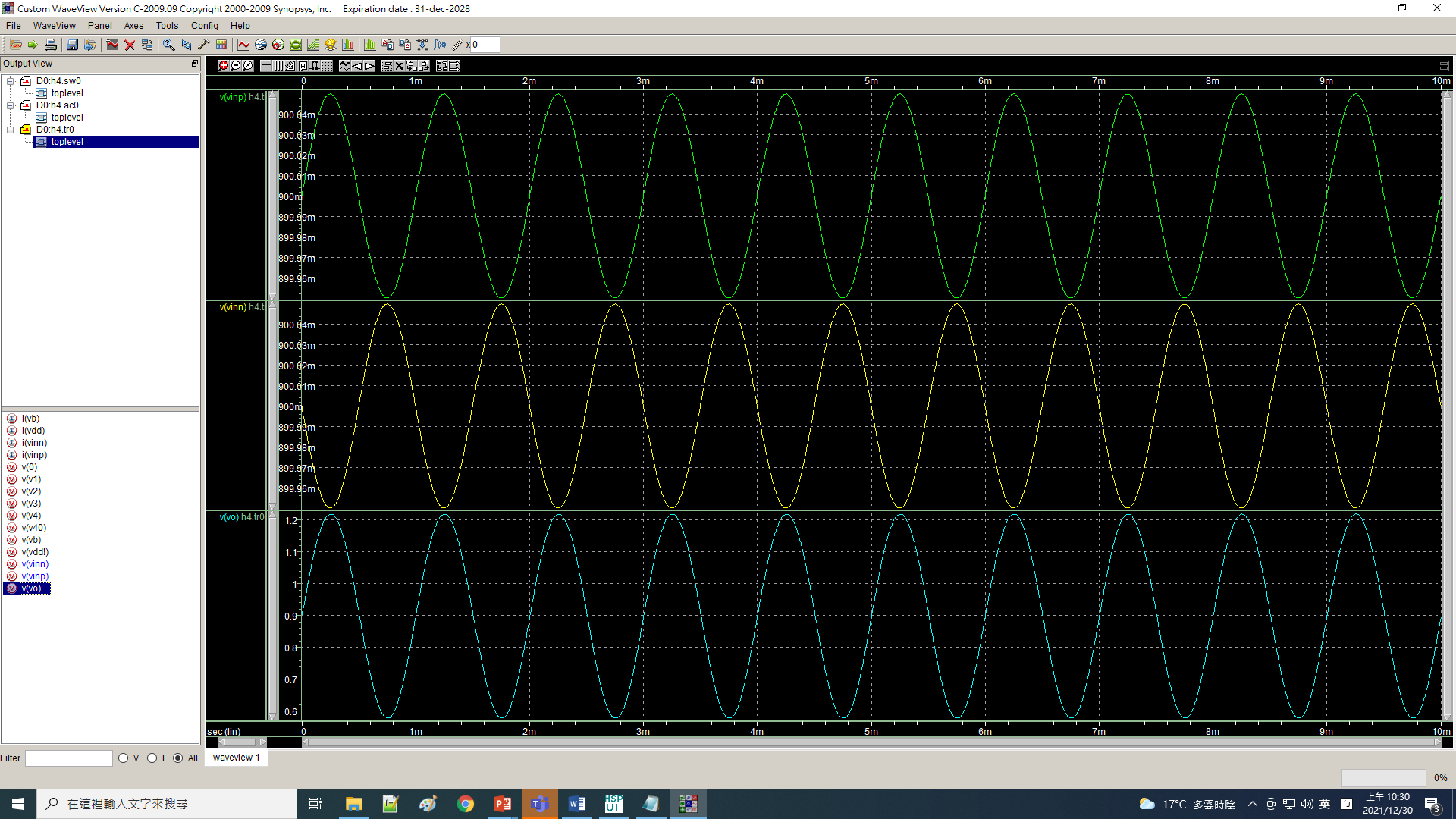
.print V(vo)

.probe ac Vdb(vo)

.end







OPA

.lib 'C:\sp\cic018.l' tt

.global gnd! vdd!

vdd vdd! 0 dc 1.8V

vss gnd! 0 dc 0

m1 v1 vb vdd! vdd! p\_18 w=0.25u l=0.18u m=1

m2 v2 v2 vdd! vdd! p\_18 w=30u l=1u m=10

m3 v4 v2 vdd! vdd! p\_18 w=30u l=1u m=10

m4 vo v4 vdd! vdd! p\_18 w=19u l=1u m=10

m5 v2 vinn v3 gnd! n\_18 w=33u l=1u m=15

m6 v4 vinp v3 gnd! n\_18 w=33u l=1u m=15

m7 v1 v1 gnd! gnd! n\_18 w=25u l=1u m=3

m8 v3 v1 gnd! gnd! n\_18 w=50u l=1u m=15

m9 vo v1 gnd! gnd! n\_18 w=22u l=1u m=10

Vb Vb gnd! DC 0.4V

Cc vo v40 5p

Rc v40 v4 1k

Vinp Vinp 0 DC 1V AC 1V sin(0.9V 0.25V 1000k)

\*Vinp Vinp 0 DC 0.9V AC 0.5V sin(0.9V 50uV 1k)

\*Vinn Vinn 0 DC 0.9V AC 0.5V 180 sin(0.9V -50uV 1k)

R1 Vinn Vo 1

\*\*analysis

.op

.option post

.option acout=0

.dc Vinp 0 1.8 0.001

.ac dec 50 1 1g

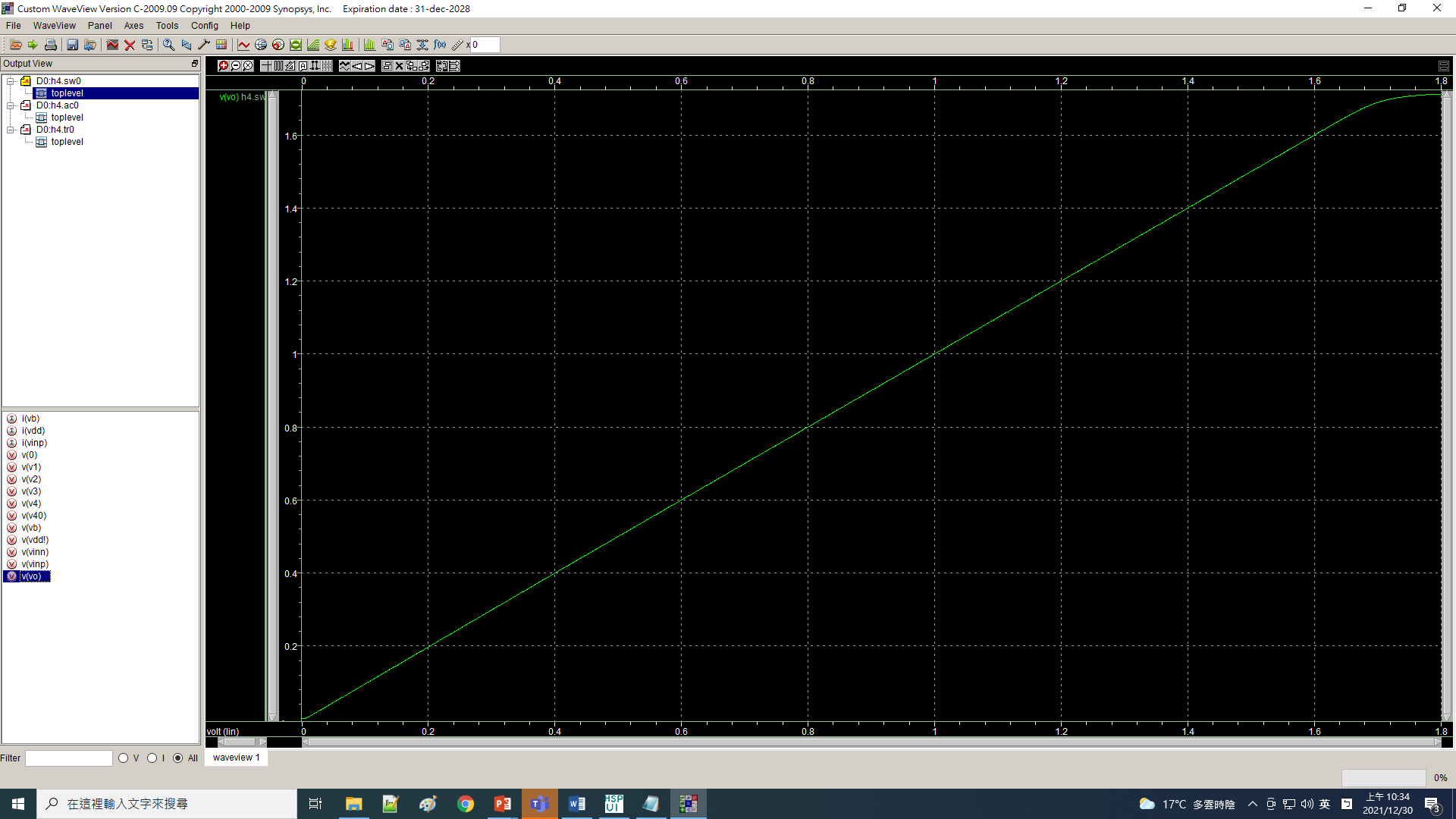
.tran 10n 10u 0 10ns

\*.tran 10n 10m 0 10us

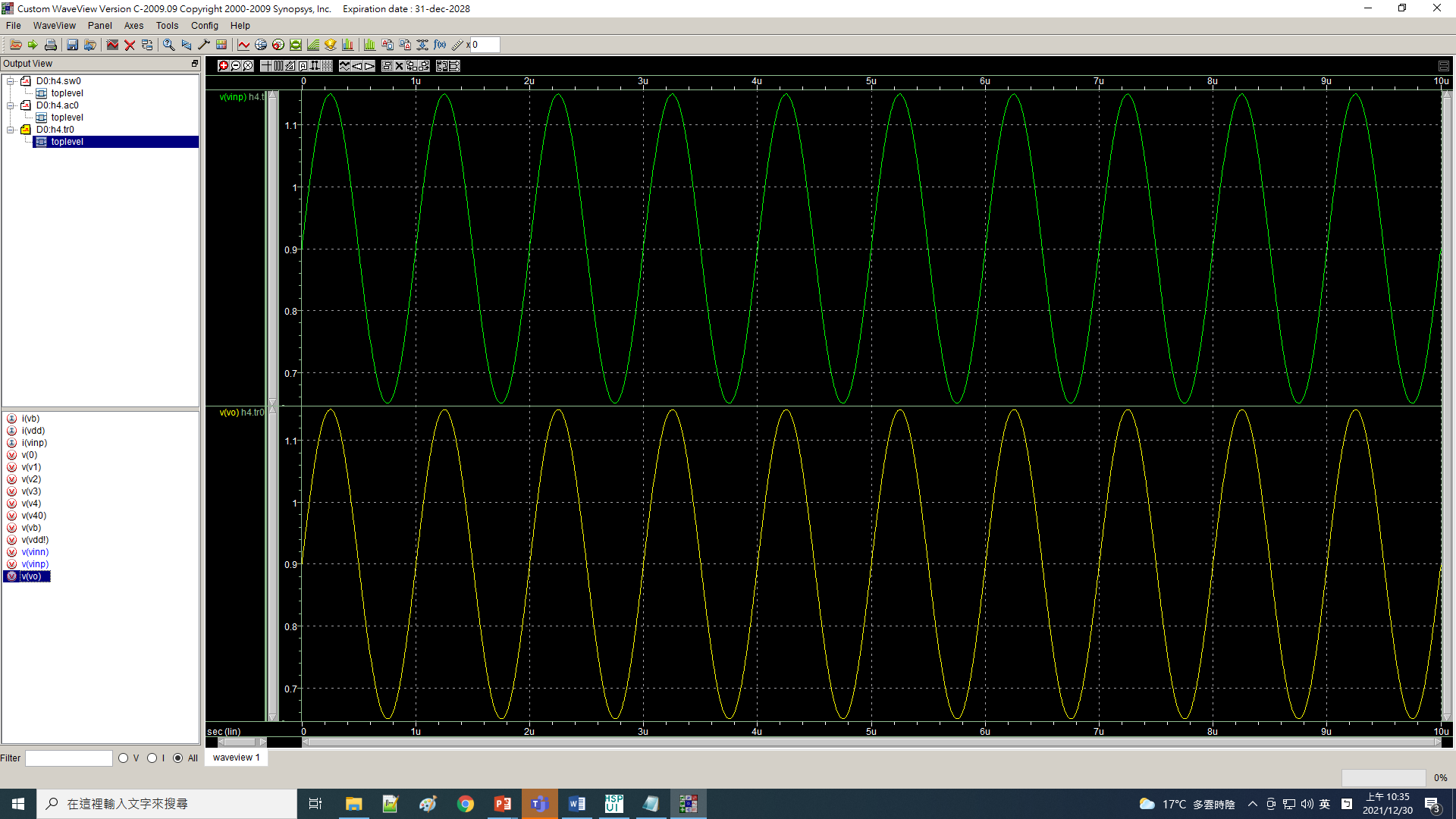
.print V(vo)

.probe ac Vdb(vo)

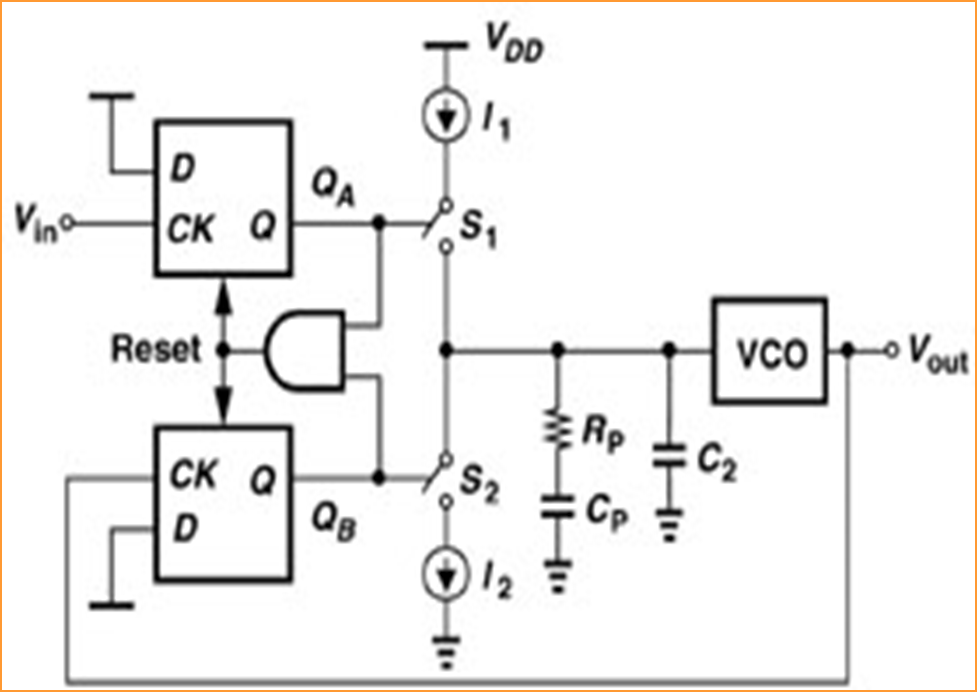
.end







**LAB8**



Frequency Synthsizer

\*\*\*\*PFD/CP/VCO\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.GLOBAL gnd vdd

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT nor2 a b y

mp1 4 a vdd vdd p\_18 w=3u l=0.18u m=1

mp2 y b 4 vdd p\_18 w=3u l=0.18u m=1

mn1 y a gnd gnd n\_18 w=1u l=0.18u m=1

mn2 y b gnd gnd n\_18 w=1u l=0.18u m=1

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT nand2 a b y

mp3 y a vdd vdd p\_18 w=3u l=0.18u m=1

mp4 y b vdd vdd p\_18 w=3u l=0.18u m=1

mn3 y a 4 gnd n\_18 w=1u l=0.18u m=1

mn4 4 b gnd gnd n\_18 w=1u l=0.18u m=1

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT inv a y

mp5 y a vdd vdd p\_18 w=3u l=0.18u m=1

mn6 y a gnd gnd n\_18 w=1u l=0.18u m=1

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT DFF ck rs q

x1 ck q 1 nor2

x2 1 2 q nor2

x3 1 3 2 nor2

x4 2 rs 3 nor2

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT PFD cka ckb qa qb

x1 cka rs qa DFF

x2 ckb rs qb DFF

x3 qa qb rs1 nand2

x4 rs1 rs inv

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT PFDCP cka ckb vb1 vb2 cp

x1 cka ckb qa qb PFD

x2 qa qab inv

mp1 4 vb2 vdd vdd p\_18 w=4u l=1u m=5

mp2 cp qab 4 vdd p\_18 w=4u l=1u m=5

mn1 cp qb 5 gnd n\_18 w=1u l=1u m=5

mn2 5 vb1 gnd gnd n\_18 w=1u l=1u m=5

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT vco vcont vout

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp1 2 2 vdd vdd p\_18 w=4u l=0.18u

mn1 2 vcont gnd gnd n\_18 w=1u l=0.18u

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp2 4 2 vdd vdd p\_18 w=4u l=0.18u m=1

mp3 5 vout 4 vdd p\_18 w=4u l=0.18u m=1

mn2 5 vout 6 gnd n\_18 w=1u l=0.18u m=1

mn3 6 vcont gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp4 7 2 vdd vdd p\_18 w=4u l=0.18u m=1

mp5 8 5 7 vdd p\_18 w=4u l=0.18u m=1

mn4 8 5 9 gnd n\_18 w=1u l=0.18u m=1

mn5 9 vcont gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp6 10 2 vdd vdd p\_18 w=4u l=0.18u m=1

mp7 11 8 10 vdd p\_18 w=4u l=0.18u m=1

mn6 11 8 12 gnd n\_18 w=1u l=0.18u m=1

mn7 12 vcont gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp8 13 11 vdd vdd p\_18 w=4u l=0.18u m=1

mn8 13 11 gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp9 vout 13 vdd vdd p\_18 w=4u l=0.18u m=1

mn9 vout 13 gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT fd fin vout

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp1 1 ffb vdd vdd p\_18 w=8u l=0.18u m=1

mp2 1 fin 2 vdd p\_18 w=1u l=0.18u m=1

mn1 2 ffb gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp3 3 fin vdd vdd p\_18 w=8u l=0.18u m=1

mn2 3 2 4 gnd n\_18 w=1u l=0.18u m=1

mn3 4 fin gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

mp4 ffb 3 vdd vdd p\_18 w=8u l=0.18u m=1

mn4 ffb fin 5 gnd n\_18 w=1u l=0.18u m=1

mn5 5 3 gnd gnd n\_18 w=1u l=0.18u m=1

mp0 vout ffb vdd vdd p\_18 w=2u l=0.18u m=1

mn0 vout ffb gnd gnd n\_18 w=1u l=0.18u m=1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.SUBCKT fd10 fin ffb

x1 fin ff1 fd

x2 ff1 ff2 fd

x3 ff2 ff3 fd

x4 ff3 ff4 fd

x5 ff4 ff5 fd

x6 ff5 ff6 fd

x7 ff6 ff7 fd

x8 ff7 ff8 fd

x9 ff8 ff9 fd

x10 ff9 ffb fd

.ENDS

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

x1 cka ckb vb1 vb2 cp PFDCP

vb2 vb2 gnd 1.2v

vb1 vb1 gnd 0.55v

Cp cp g1 50p

Rp g1 gnd 9k

C2 cp gnd 5p

x2 cp vout vco

x3 vout ckb fd10

.ic v(cp)=0 v(vout)=0

vdd vdd gnd 1.8v

vgnd gnd 0 0v

v1 cka gnd pulse(0v 1.8v 0u 0.1n 0.1n 0.5u 1u)

.op

.option post

.tran 1u 200u

.lib 'C:\sp\cic018.l' tt

.end

